

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,873,016 B2  
APPLICATION NO. : 10/678586  
DATED : March 29, 2005  
INVENTOR(S) : Park et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On Fig. 1, please replace "II" (located under RC(49)) with --II'--

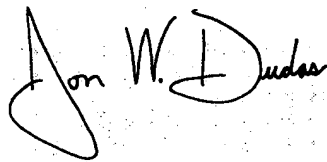
At column 5, line 1, please replace "insulation layer. 108" with --insulation layer 108.--

At column 6, line 19, please replace "semiconductor device of FIG. referring to" with --semiconductor device of FIGS. 7 and 8 is explained by referring to--

At column 8, lines 9-11, please replace claim 4 with --The semiconductor device as claimed in claim 1, wherein the conductive pattern and the resistor are horizontally aligned. --

Signed and Sealed this

Tenth Day of October, 2006

A handwritten signature in black ink, reading "Jon W. Dudas". The signature is stylized, with a large, looped "J" and a cursive "Dudas".

JON W. DUDAS  
*Director of the United States Patent and Trademark Office*